AN 18 GHz Si BIPOLAR MOLD PACKAGE PRESCALER

Masaho Mineo, Mariko Okamoto*, Kimio Hosoki*, and Hideo Ohba*
Microwave and Satellite Comm. Div./*C&C LSI Development Div.
NEC Corp.
Tsuzuki-ku, Yokohama 224-8555, JAPAN

ABSTRACT

A mold package static prescaler operating at 18GHz has been realized. The technology used is the Si bipolar process of which the emitter mask width is 0.8 μm. The cut-off frequency and the maximum oscillation frequency are 30 GHz and 40 GHz respectively. The input power range of operations is more than 10 dB in -70 to +95 °C at 1 to 15 GHz. This prescaler features a +5 V single supply voltage and 190 mW power dissipation.

INTRODUCTION

Prescalers are essential to PLL circuits that stabilize frequency of local oscillators. High speed prescalers are demanded particularly in microwave transmitters and receivers for land and satellite communications, because high speed prescalers allow direct oscillation of local oscillators and eliminate the multipliers and the filters in the multiple frequency type local oscillators. This results in smaller size and lower cost equipment.

Until now many high speed prescalers based on various kinds of device processes have been reported(for example, [1]-[3]). These are in the state of the art and mainly focus on the maximum operating frequencies and the minimum input sensitivities measured on wafers. However, in the field applications of microwave and satellite communications equipment and high speed instruments, prescalers are asked to clear the following requirements, 1)higher frequency or speed performance, 2)wide operation range in frequency and input power, 3)sufficient ambient temperature range, 4)high reliability, and to lower the manufacturing cost, 5)surface mount device that can be automatically mounted on boards.

To our knowledge, 6 GHz[4] is the maximum operation frequency of Si prescalers in market that meet all these requirements. This paper will describe our newly developed mold package 1/16 static prescaler operating at 15 GHz for commercial availability achieving the all above requirements as well.

DEVICE TECHNOLOGY

The most challenging theme of this development was to realize both the high speed operation of 18 GHz and the lower power dissipation for mold packaging at the same time. So the Si bipolar process with double-polysilicon self-aligned transistors and the trench isolation technology were used. The emitter mask width is 0.8 μm. The cut-off frequency and the maximum oscillation frequency of transistors are 30 GHz and 40 GHz respectively at Vce=1 V. By using this process, high speed, small size and low power dissipation have been achieved.

Compound semiconductor ICs have been used for high speed applications so far. But by the advances of high speed characteristics in our Si bipolar process, Si bipolar ICs can be used in these high speed applications. Furthermore, low cost ICs can be realized as Si bipolar processes are stable and allow manufacturing with a high yield rate.

CIRCUIT DESIGN

In the circuit design, parasitic capacitance of the pattern such as signal lines and bonding pads, and inductance of bonding wires and leads of package were carefully estimated and introduced into the SPICE simulations. By the study of the most appropriate values of elements such as transistor size, operating current, signal

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

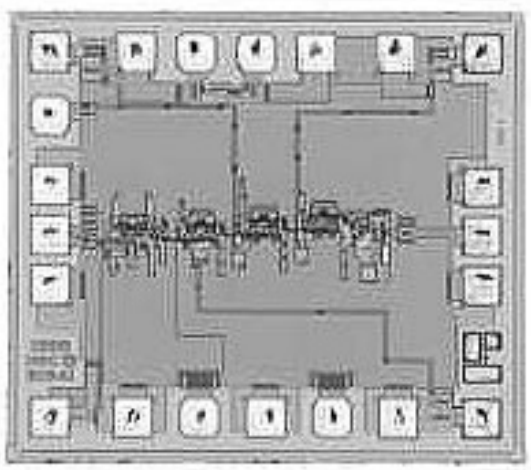

Fig.1. Chip photograph
(Chip size:1.6mm x 1.4mm)

line width, etc., the circuit was designed to achieve both high-speed operation and low power dissipation. Furthermore, since the circuit and the layout pattern are affected by each other, circuit designing and pattern designing were carried out simultaneously in reference to each other and optimized as a whole.

Figure 1 and 2 show the photographs of the chip and the block diagram of this static prescaler respectively. The circuit consists of four divide-by-two stages and an output buffer. Each divider stage includes a master-slave D-flip-flop (MS-DFF) and an inter-stage buffer. Comparing with a regenerative frequency divider[5], a static divider is used in the each stage of the prescaler, because the static divider has wide frequency range of operation as it is operable from DC in principle. This enables the IC to have many existing applications.

To reduce the power dissipation, a pre-amplifier was omitted and the MS-DFF with single emitter follower, not that with the double emitter follower, is applied to the first stage. Operation voltages of the transistors at the input were chosen so as to retain sufficient operation range of input power without preamplifier. Figure 3 shows the input sensitivity of the simulated and the measured results at the room temperature. Both results indicate good agreement. So the validity of our SPICE simulations about high frequency circuits was confirmed.

Besides a 1/16 operation, 1/8, 1/4 and 1/2 operations are available, as the second, the third and the fourth stage become a passing stage by

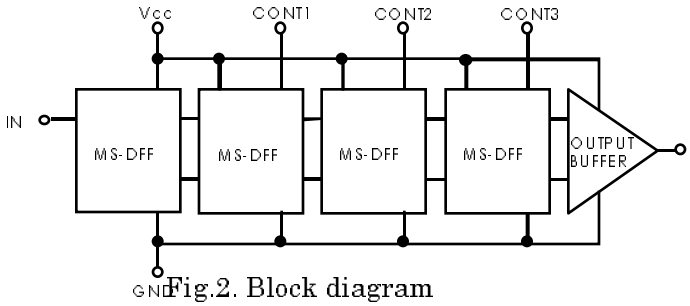

Fig.2. Block diagram

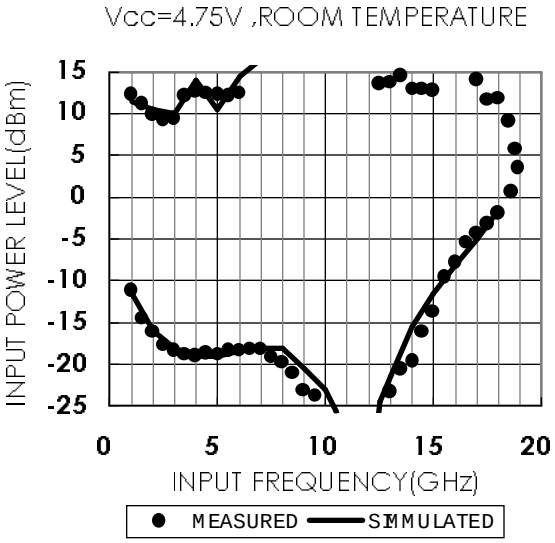

Fig.3. Simulate and measured results of input sensitivity

pulling up the control terminals. The output buffer of the prescaler can drive a 50 Ω load up to 3 GHz output frequency. This allows us to use a 3 GHz PLL IC after this prescaler. And as the results, the superior phase noise and few spurious noises of the local oscillators are expected as higher comparing frequencies are realized.

LAYOUT DESIGN AND PACKAGE SELECTION

Single-clocked input is realized by using a polysilicon electrode capacitor for RF ground of one of the differential pairs at the input. The dielectric material of the capacitor is Si_3N_4 of which the relative dielectric constant is 7.8. The

capacitance value is 2.5 pF and its area is 23 μm x 42 μm. This capacitance and additional parasitic capacitance, about 1.5 pF, make impedance low enough at 1 GHz. It was confirmed by experiments that any capacitors assembled outside the chip cannot improve the minimum input sensitivity at low frequencies.

A single ground plane of Al and a single power supply plane of Al are used in the IC. The power supply plane covers the ground plane and this makes about 20pF capacitance for bypassing. The pads for input and output are laid out to make the bonding wires being the shortest in order to reduce inductance.

As the result of lowering the power dissipation as small as 190 mW with an output power of -2 dBm, the IC chip can be assembled in a conventional mold package that is not specially customized for low thermal resistance and high speed operations. The package selected is a surface-mount type, 14 pins, shrink small outline package (SSOP) as shown in figure 4. This allows the device to be automatically mounted on boards and achieves manufacturing cost reduction. The package size is 6.2 mm x 5.4 mm including leads.

We allocated 6 leads for ground and 2 leads for power supply. As the ground plane of the IC is single, all the ground leads are in parallel. This results in reduction of inductance. The leads for power supply are also in parallel.

Fig.4. Photograph of the mold package (package size:6.2mm x 5.4mm).

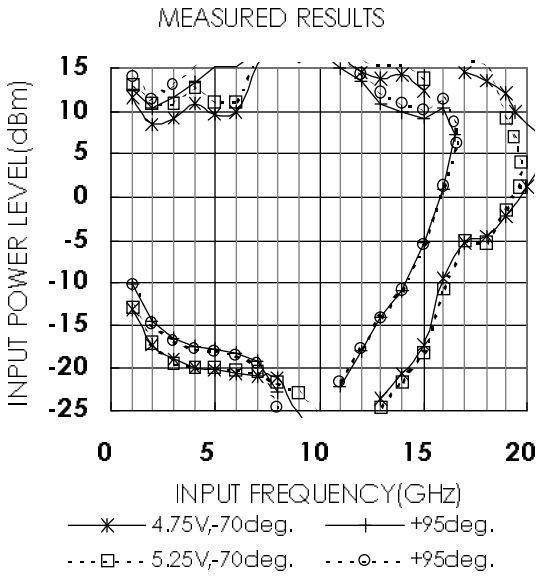

Fig.5. Input sensitivity measured at two temperatures and two voltage values.

MEASURED RESULTS

Figure 3 shows the input sensitivity versus frequency characteristics of 4.75 V power supply at room temperature. The developed unit can operate in single clocked fashion and exhibit a wide frequency range of operation from 1 to 18.8GHz at an input power level of +5 dBm. Figure 5 also shows the input sensitivities measured by 4.75 V and 5.25 V power supply at different ambient temperature together. The ambient temperature at -70 °C means that the junction temperature of the IC is under -40 °C. So cold start at -40 °C is assured, and this is sufficient for outdoor use. Achieving more than 10 dB range of input power level at 1 to 15 GHz allows the substantial applications to the prescaler.

The stable operation of this prescaler has been observed in figure 6 which shows the output waveforms in time domain. These RF measurements were done as the prescaler was mounted on a Teflon board. A blocking capacitor was used as the input DC-cut capacitor. Input power level was calibrated at the OSM connector assembled close to the IC input.

CONCLUSION

The RF performance results described so far

are summarized in Table 1 with the supply voltage and size information. In conclusion, a single-clocked, mold package static prescaler operating at 18 GHz has been realized using a Si bipolar process. These results obtained so far will give us a breakthrough to commercial availability of the high speed surface-mount prescaler.

Table 1. Performance summary.

Max. Operation Freq.	15GHz min.
Min. Operation Freq.	1GHz
Input Power Range	10dB min.
Output Power	-2dBm typ. at 3GHz
Temperature Range	-70°C- +95°C
Supply Voltage	+4.75V - +5.25V
Power Dissipation	190mW typ.
Chip Size	1.6mm x 1.4mm
Package Size	6.2mm x 5.4mm

ACKNOWLEDGEMENT

The authors are grateful to A.Sawairi and O.Tsuzuki for their contributions to this paper. They would like to express their thanks to Dr Y.Fujiki, Mr. T.Takeda and Mr. M.Mizumura for their valuable suggestions and encouragement.

REFERENCES

[1] M.Wurzer, et al., "42GHz Static Frequency Divider in a Si/SiGe Bipolar Technology," ISSCC Digest of Technical Papers, pp.122-123, Feb. 1997.

[2] Z.Lao, et al., "35-GHz Static and 48-GHz Dynamic Frequency Divider IC's Using 0.2µm AlGaAs/GaAs-HEMT's," IEEE J. Solid-State Circuits, vol. 32, No.10, pp.1556-1562, 1997.

[3] A.Felder, et al., "46 Gb/s DEMUX, 50 Gb/s MUX, and 30 GHz Static Frequency Divider in Silicon Bipolar Technology," IEEE J. Solid-State Circuits, vol. 31, No.4, pp.481-486, 1996.

[4] Technical data of HP's IFD-53010.

[5] R.H.Derksen, et al., "7.3-GHz Dynamic Frequency Dividers Monolithically Integrated in a Standard Bipolar Technology", IEEE Trans., 1988, MTT-36,(3), pp.537-541.

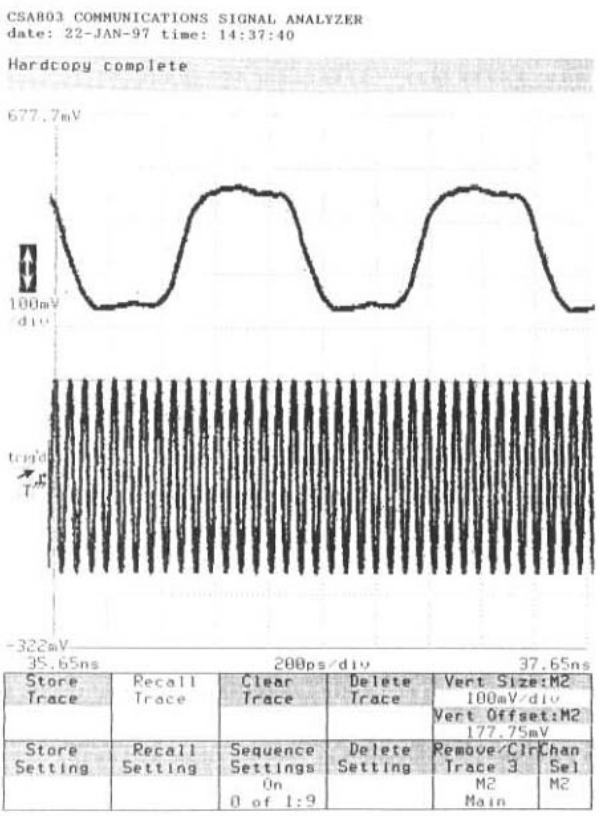

Fig.6. Input and output waveforms. Fin=18GHz, 1/16 operation